

## CLAIMS

## I CLAIM:

1. A method, comprising:  
identifying a source clock frequency having a source clock period;  
identifying a destination clock frequency having a destination clock period;  
identifying a clock gearing ratio corresponding to the source and destination clock frequencies;  
receiving a source data stream at the source clock frequency, wherein the data stream is comprised of a plurality of source data units; and  
providing the source data stream as a destination data stream at the destination clock frequency.
2. The method of claim 1, wherein the step of identifying a clock gearing ratio further comprises:  
selecting a gearing ratio from a predetermined set of gearing ratios.
3. The method of claim 1, wherein the step of providing the source data stream as a destination data stream at the destination clock frequency further comprising:  
delaying a source data unit; and  
outputting the source data unit as a destination data unit during a clock cycle associated with the destination clock frequency.
4. The method of claim 1, wherein the step of providing the source data stream as a destination data stream at the destination clock frequency further comprises:  
providing the destination data stream on a plurality of data outputs such that each received source data unit is provided as a destination data unit in the next destination clock period.

5. The method of claim 1, wherein the gearing ratio represents a first number of source clock periods that occur in substantially the same time period as a second number of destination clock periods.

6. The method of claim 1, further comprising:  
providing data representative of the clock period in which a data unit is output.

7. The method of claim 1, further comprising:  
outputting a first received source data unit as a first destination data unit in the next available destination clock period.

8. The method of claim 1, further comprising:  
outputting a first received source data unit and a second received source data unit as a first destination data unit and a second destination data unit in the next available destination clock period on a first destination output and a second destination output.

9. The method of claim 1, further comprising:  
receiving a first source data unit on a first source input and a second source data unit on a second source input;

providing the first source data unit as a first destination data unit in the next available destination clock period on a first destination output;

providing the second source data unit as a second destination data unit in a successive destination clock period on the first destination output.

10. A system, comprising:  
a first data input for receiving input data clocked by a source clock;  
a first output selector adapted to direct selected received input data to a first output as first output data;

a second output selector adapted to direct selected received input data to a second output as second output data;

a first clock gear register adapted to control the first output selector;  
a second clock gear register adapted to control the second output selector;  
wherein the first and second clock gear registers provide data representative of the destination clock periods in which data is output to the first and second outputs.

11. The system of claim 10, wherein the clock gear registers are programmable to provide customized gearing changes without system modification.

12. The system of claim 10, further comprising:  
a destination clock phase counter in communication with the clock gear registers and adapted to monitor the destination clock phase and to communicate the clock phase to the clock gear registers.

13. The system of claim 12, wherein the destination clock phase counter resets based on the status of a phase signal.

14. The system of claim 12, further comprising:  
a source clock phase counter adapted to monitor the source clock phase and to direct input data to the output selectors.

15. The system of claim 14, further comprising:  
a phase selector in communication with the source clock phase counter for identifying the source clock phase and associating input data received during a source clock phase with the source clock phase.

16. The system of claim 14, wherein the source clock phase counter resets based on the state of a phase signal.

17. The system of claim 10, further comprising a core logic unit.

18. The system of claim 10, further comprising a memory device.

19. A system, comprising:  
a first data input for receiving first input data clocked by a source clock;

a second data input for receiving second input data clocked by the source clock;

an output selector adapted to direct selected received input data to an output as output data;

a clock gear register adapted to control the output selector;

wherein the clock gear register provides data representative of the destination clock periods in which received first and second input data is output to the output.

20. The system of claim 19, wherein the clock gear register is programmable to provide customized gearing changes without system modification.

21. The system of claim 19, further comprising:

a destination clock phase counter in communication with the clock gear register and adapted to monitor the destination clock phase and to communicate the clock phase to the clock gear register.

22. The system of claim 21, wherein the destination clock phase counter resets based on the status of a phase signal.

23. The system of claim 21, further comprising:

a source clock phase counter adapted to monitor the source clock phase and to direct input data to the output selector.

24. The system of claim 23, further comprising:

a phase selector in communication with the source clock phase counter for identifying the source clock phase and associating input data received during a source clock phase with the source clock phase.

25. The system of claim 23, wherein the source clock phase counter resets based on the state of a phase signal.

26. The system of claim 19, further comprising a core logic unit.

27. The system of claim 19, further comprising a memory device.